Rare Met.
https://doi.org/10.1007/s12598-024-03147-0

RARE METALS

ORIGINAL ARTICLE

Degradation of electrical performance of few-layer tungsten selenide-based transistors

Ben-Song Wan, Run-Hui Zhou, Wen-Kai Yang, Qin Zhang, Xiang-Yu Liu, Zhi-Fu Tan, Cao-Feng Pan*, Zheng-Chun Peng*

Received: 13 May 2024 / Accepted: 1 September 2024

Abstract Semiconducting transition-metal dichalcogenides (TMDs) have garnered significant interest due to their unique structures and properties, positioning them as promising candidates for novel electronic and optoelectronic devices. However, the performance of TMDs-based devices is hampered by the suboptimal quality of metal electrodes contacting the atomically thin TMDs layers. Understanding the mechanisms that influence contact quality is crucial for advancing TMDs devices. In this study, we investigated the conductive properties of tungsten selenide (WSe_2)-based devices with different film thicknesses. Using the transmission line method, a negative correlation between contact resistance and film thickness in multi-electrode devices was revealed. Additionally, repeatability tests conducted at varied temperatures indicated enhanced device stability with increasing film thickness. Theoretical analysis, supported by thermionic emission theory and thermal simulations, suggests that the degradation in electrical properties is primarily due to the thermal effect at the contact interface. Furthermore, we found that van der Waals contacts could mitigate the thermal effect through a metal transfer method. Our findings elucidate the critical role of contact resistance in the electronic performance of 2D material-based field-effect transistors (FETs), which further expands their potential in the next generation of electronic and optoelectronic devices.

Keywords Tungsten selenide; Contact resistance; Thermal effect; Defect state; Van der Waals contact

1 Introduction

Semiconducting transition-metal dichalcogenides (TMDs) have emerged as a promising class of materials for electronic and optoelectronic devices due to their unique structure and properties [1–5]. The atomic thickness, finite bandgap, lack of free dangling bonds and excellent gate electrostatics make TMDs highly attractive for a wide range of applications in the field of nanoelectronics [6–10]. Particularly, field-effect transistors (FETs) based on TMDs have demonstrated outstanding performance characteristics such as high on/off ratio, high current density and near-theoretical subthreshold swing values. The exceptional attributes of TMD-based FETs position them as viable candidates for extremely short-channel node devices with

Ben-Song Wan and Run-Hui Zhou have contributed equally to this work.

Supplementary Information The online version contains supplementary material available at https://doi.org/10.1007/s12598-024-03147-0.

B.-S. Wan, Z.-C. Peng*
State Key Laboratory of Radio Frequency Heterogeneous Integration, School of Physics and Optoelectronic Engineering, Shenzhen University, Shenzhen 518060, China
e-mail: zcpeng@szu.edu.cn

R.-H. Zhou, W.-K. Yang, Q. Zhang, X.-Y. Liu, Z.-F. Tan, C.-F. Pan
Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing 101400, China

C.-F. Pan*
Institute of Atomic Manufacturing, Beihang University, Beijing 100191, China

Z.-C. Peng
School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China

Published online: 24 January 2025

potential implications for next-generation electronics [6, 11, 12]. However, it is of great significance to recognize that the intrinsic properties of TMDs devices are often overshadowed by contact-related issues [3, 13–17]. The atomic thinness of TMD flakes renders them susceptible to material integrity disruptions during the fabrication process [18–20], leading to the formation of high-density defect states at the contact interface between the semiconducting channel and metal electrodes. This phenomenon induces Fermi-level pinning at the contact interface and results in elevated contact resistance [3, 21–25]. The presence of energy pinning at these interfaces imposes limitations on carrier transport processes within TMDs-based devices, thereby impacting their overall electronic characteristics. Hence, addressing these challenges associated with contact properties is imperative for unleashing the full potential of TMDs materials in practical device applications.

Recently, there has been a surge in the development of alternative strategies aimed at enhancing the contact quality of TMDs devices. These strategies encompass a broad spectrum of approaches, including carrier doping with diverse metallic electrodes [26–30], the lateral metal–semiconductor–metal homogeneous epitaxial junction via phase engineering [30–34], the establishment of van der Waals contacts through transfer metal [18, 35, 36] or semimetal [37–40], and the minimization of the contact area by edge contacts [41–44]. The primary objective behind these strategies is to either reduce the conducting area or enhance the effective carrier concentration at the contact interface, which is crucial for facilitating the transition of carriers across the Schottky barrier and forming low-resistance contacts with TMDs semiconductors. Furthermore, to tackle the issue of contact resistance and its influence on device stability, researchers have delved into the complex carrier transport mechanisms at the contact interface. It has been noted that when carriers traverse the Schottky barrier, numerous factors come into effect, influencing the generation and reduction of contact resistance. These factors encompass not only thermal effects but also interface scattering and impurity scattering, all of which contribute to the overall electrical performance of devices. Moreover, as an integral part of the ongoing investigations, considerable attention has been focused on comprehending the impact of diverse surface treatments and material structures on the carrier behavior at the contact interface [45, 46]. This all-encompassing approach is aimed at uncovering potential strategies for minimizing contact resistance and optimizing device stability. Additionally, it is essential to contemplate the potential transformation of these discoveries into practical applications within electronic devices. The repeatability of electrical performance is a crucial factor in guaranteeing reliable functionality over an extended period. Hence, by attaining a profounder understanding of the fundamental mechanisms governing contact resistance and its implications for device stability, those researchers are paving the way for advancements in electronic engineering and materials science.

In this study, the WSe_2 was selected to investigate the contact properties of TMDs devices with different layers. Different layers of WSe_2 were synthesized through a vapor-phase evaporation approach, enabling us to systematically explore the impact of film thickness on device performance. Subsequently, multi-electrode devices on different layers were fabricated to acquire contact resistance based on the transmission line method (TLM). The above-mentioned fabrication process involved precise nanoscale patterning and deposition techniques to ensure accurate measurement of electrical characteristics. The acquired data provided valuable insights into the interfacial behavior between metal contacts and TMDs at varied film thicknesses. Following this, repeatability tests under variable temperatures were conducted to disclose the stability of electrical characteristics for devices with different layers. These tests involved rigorous temperature cycling and measurements to assess the reliability and robustness of TMDs-based devices operating conditions. Then, to elucidate the degradation of electrical properties observed in different layers, revised thermal-electron emission theory and thermal simulation were employed. These theoretical frameworks provided a deeper understanding of electron transport mechanisms within TMDs at elevated temperatures, shedding light on fundamental aspects that governed device performance. Finally, the electrical properties of van der Waals (vdw) contact devices obtained by the metal transfer method were demonstrated. This demonstration showcased an alternative approach for achieving low-resistance contacts in TMDs-based electronics, offering potential solutions for enhancing device performance. Overall, this work provides fundamental insights into uncovering the degradation of electrical performance in TMDs devices with different layers and offers valuable guidance for optimizing fabrication processes and design strategies for 2D electronic devices.

2 Experimental

2.1 Synthesis of WSe_2 flakes, device fabrication and measurement

The WSe_2 flakes were synthesized in a chemical vapor deposition (CVD) system using thermally evaporated vapor-phase methods at atmospheric pressure via a sequential growth process. WSe_2 powder (99.99% purity) served as the volatile source for the synthesis process.

Initially, the powder was placed in a quartz boat at the center of the heating zone of the tube furnace, with a 1-inch quartz tube utilized as the vapor tunnel. The SiO_2 (300 nm)/Si substrate was positioned at the downstream end of the heating zone as the synthesis substrate. Subsequently, the heating zone was heated to high temperatures under ambient pressure, with an argon gas flow of ~ 50 sccm. The growth period was maintained for about 7 min. After the heating process, the furnace was allowed to cool naturally. The thickness of WSe_2 flakes exhibited a positive correlation with the heating temperature. The vaporization temperatures for monolayer, bilayer, and multilayer WSe_2 flakes were ~ 1100, ~ 1130 and >1150 °C, respectively. The thickness of the synthesized WSe_2 flakes was characterized by atomic force microscopy (AFM, MFP-3D-SA). Raman and Photoluminescence (PL) spectra were measured using a laser confocal micro-Raman system (LabRAM HR Evolution), with an excitation laser wavelength of 532 nm and a total laser power attenuated to 5%. For device fabrication, electron beam lithography was first employed to create marks on the SiO_2 (300 nm)/Si substrate with electron beam resist polymethyl methacrylate (PMMA) on the WSe_2 flakes. An optical microscope was used to accurately locate the WSe_2 flakes. Subsequently, 5 nm/45 nm Cr/Au was deposited as the drain and source electrodes after micropatterning using electron beam lithography. Finally, acetone was used to remove the excess resistance during the lift-off process. The electrical characteristics were measured using a Keithley 4200 system, and a vacuum probing station was utilized for high vacuum measurements. A temperature-changeable measurement system was employed to assess properties at variable temperatures, using liquid nitrogen as the coolant.

2.2 Metal transfer methods of WSe_2 vdw devices

We first prepared 40-nm-thick metal electrodes (Ag and Au) on a silicon substrate using ultraviolet lithography and magnetron sputtering methods. Next, polystyrene (PS) was spin-coated on top of the metal electrodes. A layer of polydimethylsiloxane (PDMS) colloidal sol was subsequently hand-coated on the PS/Si substrate. Owing to the hydrophobicity and viscosity of the PS film, the PS layer exhibited weak adhesion to the Si substrate and could be mechanically released by placing it in deionized (DI) water. The PS/PDMS film was then align-transferred onto the synthesized WSe_2 flakes on a SiO_2 (300 nm)/Si substrate using point-to-point transfer equipment. Following this, the SiO_2 (300 nm)/Si substrate was heated to 95 °C to peel off the PDMS film. Finally, dimethylformamide (DMF) liquid was used to remove the residual PS film, with the process being repeated twice. Figure S1 shows schematic illustrations of the metal transfer method.

3 Results and discussion

3.1 Comprehensive characterization of the optical properties of WSe_2 flakes

The WSe_2 flakes were synthesized through thermal evaporation at atmospheric pressure within a vapor deposition process, utilizing high-purity WSe_2 powder (99.99%) as the vapor-phase reactant. This approach could ensure the generation of high-quality monocrystalline WSe_2 flakes featuring remarkable uniformity and size, as depicted in Fig. 1a. The synthesis procedure entailed heating the WSe_2 powder to temperatures exceeding 1100 °C, leading to its vaporization under the flow of argon, which served as both a carrier gas and provided a protective atmosphere. Subsequently, the vaporized WSe_2 was adsorbed onto a SiO_2/Si substrate located at the downstream end of the heating zone, where it underwent nucleation and growth to form monolayer WSe_2 flakes. The optical image in Fig. 1a disclosed that these synthesized monolayer WSe_2 flakes could attain sizes of ~ 100 μm, demonstrating extraordinary uniformity across their dimensions. To monitor the thickness of these synthesized flakes, an AFM was employed. As shown in Fig. S2, the thicknesses of the monolayer, bilayer and trilayer structures were ~ 1.2, 2.5 and 3.6 nm, respectively. Moreover, detailed height profiles suggested that these periodic thicknesses were consistent throughout all the synthesized WSe_2 flakes. These experimental particulars offered valuable insights into our capacity to precisely control both size and thickness during synthesis processes while ensuring high quality and uniformity in our resultant materials. In the photoluminescence (PL) spectrum presented in Fig. 1b, the characteristic luminescence peak of the synthesized WSe_2 flakes exhibited a notable redshift toward longer wavelengths as the thickness increased. The peak wavelength shifted from 774.1 nm for the monolayer to 791.5 nm for the bilayer and 791.8 nm for the trilayer, indicating an increase in wavelength shift of up to 17.7 nm when comparing the monolayer with the trilayer WSe_2. Moreover, the luminescence intensity of the monolayer was ~ 48,000, but it underwent a marked decrease for the bilayer (~ 5400) and the trilayer (~ 1,140). The luminescence intensity showed a distinct negative correlation with the thickness under the same laser irradiation. Additionally, an extra luminescence peak at approximately 850 nm existed in the spectra of the bilayer and trilayer flakes, suggesting additional excitonic luminescence in these thicker layers beyond the recombination luminescence observed in the monolayer WSe_2. As the number of layers of the WSe_2 flakes increases, the mobility of electrons and holes is enhanced, the quantum confinement effect weakens, and simultaneously, the interlayer coupling effect strengthens along with the growth in the

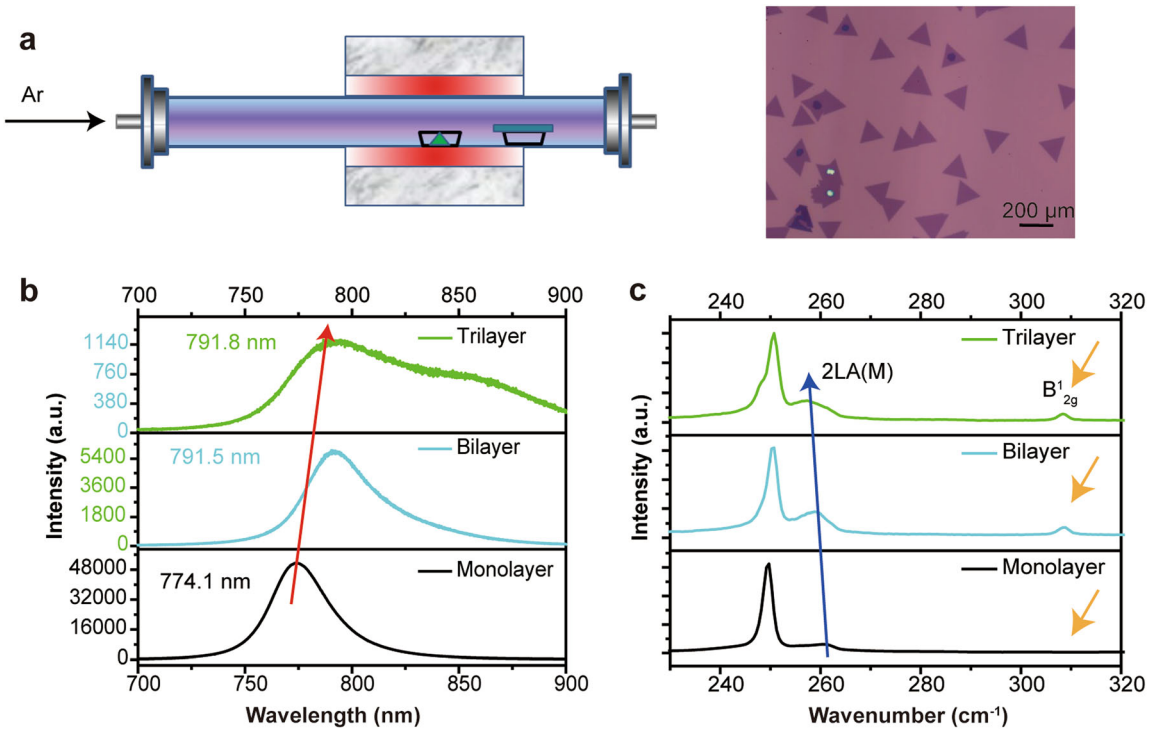

Fig. 1 Optical image and spectra information of synthesized WSe_2 flake: **a** schematic diagram of tube furnace (left) and optical image of WSe_2 flakes (right) on Si/SiO_2 substrate; **b** PL spectra of different layers WSe_2 flake (red arrow represents red shift of peak position with different layers); **c** Raman spectra of different layers WSe_2 flake (blue arrow points out evolution of second-order vibration versus different layers, and orange represents transformation of interlayer vibration B^1_{2g})

number of layers. This leads to the reduction of the bandgap value of the material as the number of layers expands, causing the redshift phenomenon in the PL spectrum. Meanwhile, when the number of layers of WSe_2 increases, its bandgap type will also change from a direct bandgap to an indirect bandgap. This transformation hinders the direct absorption or emission of photon energy and triggers phonon excitation, resulting in a decreased luminescence intensity. Figure 1c presents the Raman characteristics of distinct layers of WSe_2, with wavenumbers ranging from 230 to 340 cm^{-1}. The characteristic vibration modes, 2LA(M) and B^1_{2g} represent the in-plane vibration, second-order vibration caused by longitudinal acoustic phonons, and interlayer vibration, respectively. It was intriguing to note that while the in-plane vibration E^1_{2g} remained unaltered across diverse layers, there was a discernible shift in the peak position of the second-order vibration 2LA(M) towards lower wavenumbers, with a significant shift of up to approximately 4 cm^{-1} between the trilayer and monolayer. Additionally, the Raman intensity increased significantly with thickness. This phenomenon could be attributed to the alterations in interlayer forces and crystal structure resulting from interlayer coupling effects. These changes give rise to variations in both peak shifting and intensity enhancement of specific vibrations such as 2LA(M), providing valuable insights into how these properties evolve with film thickness. Furthermore, the interlayer vibration B^1_{2g} at 308.1 cm^{-1} disappears in the Raman spectrum of the monolayer, which is caused by the lack of van der Waals forces between interlayers. Additionally, the PL and Raman mapping images of monolayer WSe_2 shown in Fig. S3 revealed symmetrical mapping images, demonstrating that vapor-phase synthesized WSe_2 flakes exhibited excellent optical characteristics.

3.2 Characterization of electrical properties of WSe_2 devices with different layers

The analysis of the spectrum further revealed that the interlayer coupling effects exerted a critical role in influencing the vibrational characteristics of WSe_2 across various layers. Notably, when transitioning from the monolayer to the trilayer, the contact resistance was measured using the TLM to explore the contact properties of WSe_2 devices with different layers. A multi-electrode structure composed of 5 nm/45 nm Cr/Au electrodes was successively deposited as the drain and source electrodes on WSe_2 flakes through electron beam lithography. Further fabrication details were provided in the Experimental

section. As depicted in Fig. 2a, the channel length between adjacent electrodes in multi-electrode devices was variable, enabling us to obtain electrical properties for diverse channel lengths by choosing different electrode pairs. The total resistance of a FET device could be decomposed into contact resistance (R_c) and channel resistance (R_L). The schematic illustration of the resistance distribution is presented in Fig. 2b. R_c corresponds to the resistance that charge carriers encounter during the thermal emission process, which is mainly influenced by defect density and carrier scattering at the metal–semiconductor interface. This value has a positive correlation with the contact area. Conversely, R_L represents the channel resistance of the semiconductor between the drain and source electrodes, which can be modulated by the gate voltage. It mainly relies on the carrier density of the semiconductor, as well as the channel length and width of the FET device. For a uniform single-crystal FET device, when the channel length is reduced to zero while keeping the channel width constant, the total resistance approximates R_c. Thus, linear regression can be utilized to determine R_c from the relationship between resistance and channel length. A typical transfer curve on a linear scale for multi-electrode monolayer devices was depicted in Fig. 2c. The channel lengths between adjacent electrodes were set at 4, 7, 10, 13 and 16 μm, and by selecting any two electrodes, 15 devices with diverse channel lengths but uniform channel widths could be obtained. The transfer results revealed that all devices exhibited P-type semiconducting behavior and operated in depletion mode with low quiescent power dissipation. The on/off ratio derived from the semilogarithmic transfer curve amounted to 10^9, indicating

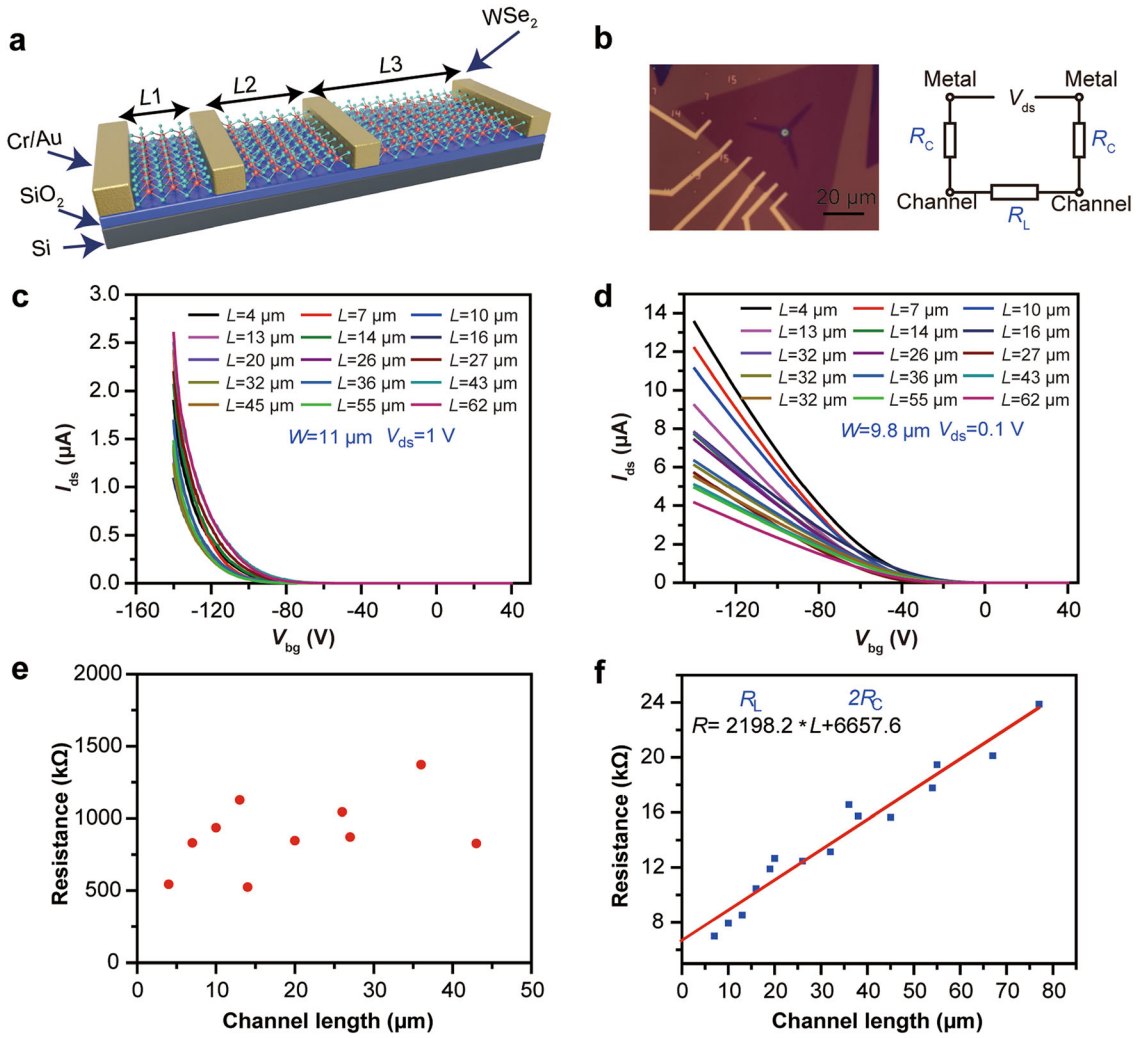

Fig. 2 Electrical properties of multi-electrodes devices on monolayer and bilayer WSe_2 flakes: **a** schematic image of multi-electrode FET devices; **b** typical optical image of a muti-electrode monolayer WSe_2 FET; transfer properties of monolayer and bilayer WSe_2 FET with different channel lengths: channel width of device and V_{ds} is: **c** 11 μm and 1 V, **d** 9.8 μm and 0.1 V; resistance statistics of multi-electrodes monolayer WSe_2 FET at **e** V_{ds} = 1 V, **f** V_{ds} = 0.1 V and V_{bg} = − 140 V with different channel length

notable gate electrostatics in the fabricated devices. Nevertheless, the current (I_{ds}) between the drain and source electrodes in monolayer devices experienced exponential growth as the gate voltage (V_{bg}) swept from positive to negative, failing to reach saturation. This phenomenon indicates severe carrier scattering at the contact interface, resulting in performance degradation under voltage gating. In Fig. 2d, the channel lengths between consecutive electrodes for bilayer devices were set at 4, 7, 10, 13 and 16 μm. In contrast to monolayer devices, the I_{ds} for bilayer devices experienced a transition from exponential to linear increase along with V_{bg} swept, suggesting a superior contact interface quality compared to monolayer devices. The total resistance, which was computed by the ratio of V_{ds} to I_{ds} versus channel length, was summarized to determine the contact resistance under a gate voltage bias of −140 V. Figure 2e, f presents the resistance statistics for monolayer and bilayer devices, respectively, which were derived from the transfer curves in Fig. 2c, d. The resistance of monolayer devices exhibited a scattered distribution with respect to the channel length, making it challenging to extract contact resistance from this relation. In contrast, the resistance of bilayer devices exhibited a well-defined correlation with channel length. By employing the least squares fitting method, the R_c for bilayer devices was found to be ∼ 6657.6 Ω, comparable to the reported values for WSe_2 devices, with R_L showing a proportionality factor of 2198.2 in relation to the channel length. In Fig. S4a, the contact properties of trilayer devices were also examined by employing TLM, revealing an R_c of 5603.3 Ω under a gate voltage bias of −140 V. Additionally, the R_c values under different gate voltage biases were illustrated in Fig. S4b, indicating that the contact resistance was independent of R_L. Considering the contact resistance at the interface, the voltage bias imposed on the semiconductor channel was effectively reduced when the current flowed through the circuit. Thus, the actual voltage bias (V_{ds}') on the semiconductor channel was calculated as $V_{ds}' = V_{ds} - I_{ds} \times R_c$. The relationship between V_{ds}' and channel length under V_{bg} values of −140, −135 and −130 V is shown in Fig. S4c. The results revealed that the proportion of contact resistance decreased with the increase in channel length and showed minimal variation under different V_{bg} values. Furthermore, a comprehensive comparative analysis was carried out on the data obtained from our advanced devices and those presented in other relevant studies, as illustrated in Table S1. This scrupulous comparison not only validates the extraordinary electrical properties of our fabricated devices but also offers valuable insights into the performance disparities between diverse fabrication approaches. The results evidently suggest that our bilayer and trilayer materials, elaborately fabricated via physical vapor deposition (PVD), showcase significantly higher on-state currents when contrasted with those produced through mechanical exfoliation. Additionally, it is remarkable that the contact resistance of our multi-electrode devices is relatively lower than that of others, which can mainly be attributed to the extremely high crystal quality of the synthesized materials.

To further elaborate on the phenomenon of contact resistance in monolayer devices, it is of paramount importance to delve into the complex factors that exert an influence on the contact performance of these devices. The contact performance of FET devices is acknowledged to be predominantly governed by carrier scattering within the substrate and interface contact. In the case of two-dimensional WSe_2 featuring an intrinsic doping concentration of $\sim 1.26 \times 10^3$ cm^{-2} and a high Schottky barrier height (SBH) in the fabricated devices, it becomes manifest that interface contact plays a crucial role in determining the contact properties of WSe_2 devices. During the fabrication process, metal electrodes were painstakingly deposited onto WSe_2 flakes through electron beam evaporation, as depicted in Fig. 3a. Under the bombardment of electron beams, metal atoms vaporize and subsequently impinge upon the surface of WSe_2 flakes with high energy. The robust covalent bonds between metal atoms and semiconductor atoms cause substantial damage to the WSe_2 surface, giving rise to a defective layer characterized by interstitial atoms, substitute atoms, vacancies, metal infiltrating atoms and other interface states. These defects exert a profound influence on the transport properties of the devices. This process brings about a modification in the electronic structure of WSe_2 at the atomic level. The introduction of interstitial and substitute atoms generates localized states within the band gap, influencing charge carrier mobility and recombination dynamics. Additionally, vacancies serve as scattering centers for charge carriers, resulting in increased resistivity and diminished device performance. In Fig. 3b, 17 repetitive scans were presented for a monolayer device. The outcomes revealed that the device manifested outstanding gate electrostatics during the initial test, with the on-current (I_{on}) attaining ∼ 3 μA under $V_{bg} = -140$ V and $V_{ds} = 0.1$ V. As the number of tests escalated, the I_{on} of the device gradually decreased, plummeting to merely 0.04 μA at the 17th measurement, indicating a reduction of two orders of magnitude compared to the initial value. This alteration in current suggests that the electrical properties of the monolayer device are unstable upon repeated testing. The inset figure depicted the corresponding fitting curves of I_{on} versus measurement number, revealing that the test results could be precisely fitted with an exponential equation $y = a \times e^{\frac{b}{x+c}}$. The variation of I_{on} demonstrates an exceptionally excellent correspondence with this equation. The

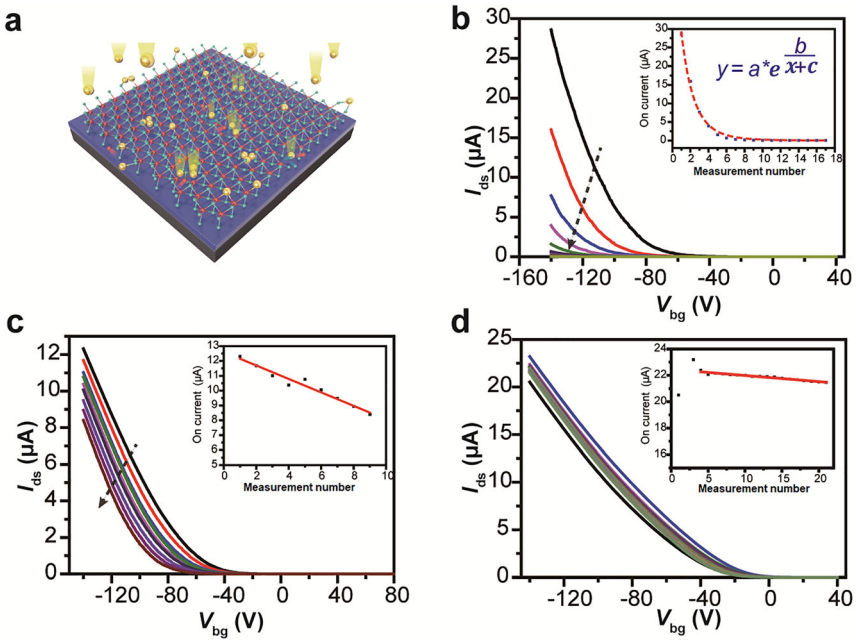

Fig. 3 Comparison of different layers WSe_2 FETs under repeatability test (room-temperature transfer curves are measured upon V_{bg} sweeping from −140 to 40 V in steps of 0.5 V and V_{ds} = 0.1 V): **a** schematic diagram of metal atom evaporation; **b** typical transfer curves of a monolayer WSe_2 device under 17 times repeatability measurement and (inset) exponential variation of I_{on} versus n (black dash line represents fitted exponential equation); **c** typical transfer curves of a bilayer WSe_2 device and (inset) linear variation of I_{on} versus n; **d** typical transfer curves of a trilayer WSe_2 device and (Inset) stabler linear variation of I_{on} versus n

results of the repeatability test for bilayer and trilayer devices were presented in Fig. 3c, d. In contrast to the monolayer device, the bilayer and trilayer devices exhibited conspicuously higher stability. The electrical performance of the bilayer device, depicted in Fig. 3c, is slightly attenuated with an escalating number of measurements. The inset figure indicated that I_{on} decreased from 12.3 to 8.2 μA after 9 measurements, presenting a slight linear decrease in relation to the number of measurements. The repeatability test result of the trilayer device is shown in Fig. 3d. Compared with thinner-layer devices, the trilayer device exhibited higher stability, with nearly no alteration in transfer properties even after 20 measurements. The inset figure illustrated the variation of I_{on} in relation to the number of measurements, suggesting that the value of I_{on} did not attenuate with increased test times. Among all the devices, it is obvious that device stability significantly augments with thickness. This result can be elucidated by introducing interface state energy into the bandgap theory of FET devices. The schematic bandgap diagram is shown in Fig. S5. According to the thermionic emission process in equilibrium, the emission current of the FET device can be expressed by the thermal-electron emission formula:

$$I = AA^*T^2e^{-\frac{q\phi_{BP}}{kBT}} \quad (1)$$

where A and A^* represent the area of contact interface and Richardson constant, k_B and T represent the Boltzmann constant and temperature, q represents the electric charge of an electron, ϕ_{BP} represents the value of SBH. According to the formula, the current is strongly correlated with the SBH at the contact interface, which is associated with the energy levels of the semiconductor and metal. Nevertheless, the presence of interface states gives rise to a pinning effect on the energy levels at the interface, leading to variations in the channel current. When taking the interface states into account, the current will be adjusted as follows:

$$I = A'A^*T^2e^{-\frac{qb}{kBT}}\left(e^{-\frac{q\phi m}{kBT}}\right)^{\frac{\varepsilon i}{q\delta DS-\varepsilon i}} \quad (2)$$

Here, the right part indicates the impact of interface states on current, where D_S represents the density of interface states per unit area and energy interval, ε_i and δ represent the permittivity and thickness of insulating layer, respectively. The specific derivation process is presented in Fig. S5. Considering the bombardment during the metal evaporation process, high-density defects arise at the interface between electrodes and the semiconductor. The existence of these defects enhances the SBH at the interface, thereby lowering the injection efficiency of carriers. Simultaneously, as carriers pass through the barrier, their interaction with these defects causes scattering, modifying their original energy and momentum. This reduces the effective transmission distance and lifetime of carriers, resulting in large contact

resistance and a high voltage drop at the contact interface, when carriers flow across the interface, excessively high thermal effects may arise at the minute contact interface, activating and exacerbating defect states. This phenomenon deteriorates with the increase in measurement numbers. Owing to the ultrathin nature of the monolayer, the flake becomes more vulnerable to atomic bombardment, leading to a higher density of defect states and higher contact resistance. This impedes the emission efficiency of carriers during the thermionic emission process, giving rise to instability in electrical performance and exponential degradation of the on-current. For multilayer WSe_2, the damaged surface layer can safeguard the underlying layers from further harm by metal atoms, subsequently demonstrating lower defect density and contact resistance. As a result, the thermal effects are mitigated compared to monolayer devices, leading to greater stability.

3.3 The stability of WSe_2 device varies with temperature

As widely acknowledged, the electrical characteristics of semiconductors are highly sensitive to temperature. At low temperatures, the impact of electron scattering, interface flaws, and surface defects is mitigated. Consequently, low-temperature experiments were conducted to validate the effect of contact resistance on the electrical performance of diverse layers. The repeatability tests of the electrical properties of devices with different layers under varying temperatures are illustrated in Fig. 4. The repeatability tests were carried out 16 times at each point, with the temperature ranging from 150 to 280 K in increments of 10 K, and statistical information of I_{on} was acquired from the repeatability transfer curves under distinct conditions. The schematic diagrams of monolayer, bilayer and trilayer WSe_2 transistors were depicted in Fig. 4a–c, respectively. Additionally, the 3D bar maps in Fig. 4d–f depicted the I_{on} measurement number in relation to temperature for monolayer, bilayer and trilayer devices, respectively. Furthermore, to facilitate a more favorable comparison of the results, we presented the logarithmic outcomes of the 3D bar maps in Fig. S6. Concerning the monolayer device in Fig. 4d, the initial value of I_{on} was 3 μA. When the temperature was below 190 K, although the on-state current value fluctuated to a certain extent, it remained relatively stable, typically ranging from 2.5 to 3 μA. However, when the temperature exceeded 190 K, I_{on} underwent a sharp decline with the increase in measurement numbers. This decreasing pattern was somewhat similar to that in Fig. 3. When the temperature rose to 210 K, the current underwent a sharp attenuation, with the value reducing from the order of magnitude of 10^{-6} to 10^{-8}. At 220 K, it attenuated to approximately 10 pA, and I_{on} reduced to a minimum value within the picoampere range when the temperature exceeded 230 K (Fig. S7a). At this juncture, the on-state current value of the device persists at the pA level, demonstrating no significant fluctuations and suggesting that the device has sustained damage and is no longer capable of functioning normally. The I_{on} statistical information of the bilayer in relation to temperature is presented in Fig. 4e. Comparable to the results of the monolayer device, the on-state current value of the bilayer device also maintained high stability at low temperatures. The

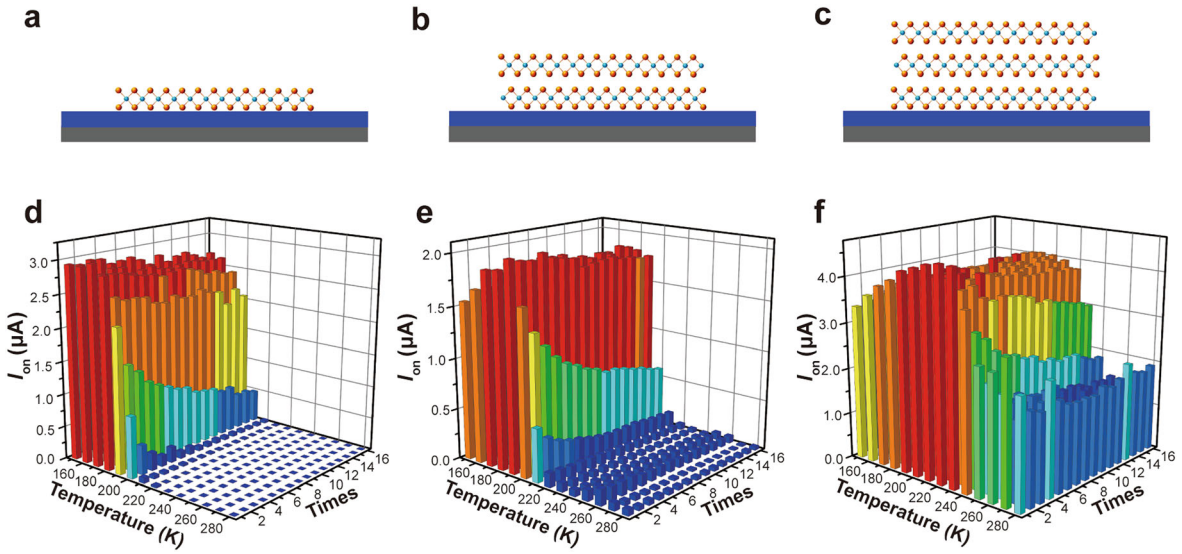

Fig. 4 Electrical properties of different layers WSe_2 devices at variable temperature: diagrammatic drawing of different layers WSe_2 transistors of **a** monolayer, **b** bilayer and **c** trilayer; 3D bar maps of I_{on}-n versus temperature of **d** monolayer, **e** bilayer and **f** trilayer WSe_2 devices

disparity lay in that I_{on} of bilayer device commences to deteriorate from 200 K, and the deterioration tendency was notably slower than that of the monolayer. At 200 K, the value deteriorated from ~ 1.5 to 0.5 μA. At 210 K, it decayed to the order of 10^{-7}, and at 220 K, it decayed to ~ 6×10^{-8}. Thereafter, the I_{on} of the device fluctuated around this value without any alteration in the order of magnitude. In the transfer curve results presented in Fig. 4f, it could be noticed that as the test temperature kept rising, although the on-state current of the device decayed to a certain extent, the device could still function normally, with an on–off ratio reaching the order of 10^{-6}. Unlike monolayer and bilayer devices, trilayer device exhibited even greater stability. When the test temperature was lower than 230 K, the on-state current value of the trilayer device remained consistently between 3.5 and 4 μA. As the temperature rose to 230 K, the current of the device started to show a more significant decay, decreasing from 3.5 to 3 μA. At 240 K, it decayed to ~ 2 μA. Subsequently, as the temperature kept rising, the on-state current of the device fluctuated between 2 and 2.5 μA under multiple repetitive tests. The typical transfer curves shown in Fig. S7c indicated that the maximum and minimum values of I_{on} varied from 4.3 to 2.5 μA within the temperature range from 150 to 280 K during multiple measurements. Simultaneously, after multiple repetitive tests, the device still maintained an on–off ratio as high as 10^9 at the room temperature of 280 K, manifesting extremely high stability compared to monolayer and bilayer devices. The results reveal that the electrical properties of WSe_2 have a high correlation with temperature, where the thermal effect plays a crucial role in activating interface states and influencing the electrical properties. Figure S8 and the extended thermal simulation video presented the thermal effect simulation at the contact interface. It could be observed that owing to the large SBH at the contact interface, the equivalent contact resistance was significantly higher than the channel resistance, causing excessive Joule heat for carrier flows along the circuit. This results in a higher temperature at the drain electrodes and source electrodes compared to the channel material [47], with the increase in the relaxation time (the total simulation time is carried out to 1000 μs), the high-temperature heat at the source and drain electrodes will gradually be transferred to the channel material and the atmosphere, resulting in thermal dissipation from the contact interface to the channel material. When the heat generation rate and dissipation rate reach equilibrium, the temperature between the metal electrodes and the channel materials will tend to be consistent and maintain a stable value at this time. Compared with monolayer WSe_2, the thermal dissipation rate of trilayer WSe_2 has an advantage over monolayer due to the heat conduction between interlayers, leading to the fact that the multilayer devices are less affected by the heating effect, and the device exhibits higher stability. In contrast, considering that the SiO_2 substrate is a poor thermal conductor, monolayer molecules make it difficult for the monolayer device to transfer the heat to the outside environment. In a lower-temperature environment, the heat can be effectively dissipated as the coolant flows around the testing environment, resulting in stable electrical performance. However, with the increase in the environmental temperature to over 190 K, the poor thermal conduction causes the temperature at the contact interface to increase, and the particle collision under high temperature will further permanently destroy the crystal structure of the monolayer semiconductor, resulting in cumulative contact resistance and unrecoverable electrical performance. For the bilayer devices, their heat dissipation condition falls within the range between that of the trilayer and monolayer devices. Concerning the monolayer devices, when the temperature exceeds 190 K, the devices lose thermal equilibrium. The defect density at the interface gradually ascends with the increment of the test times, eventually leading to damage to the material. In contrast, the bilayer devices lose thermal equilibrium approximately at 210 K. Nevertheless, differing from the monolayer ones, its bilayer nature allows the material to have a certain heat dissipation effect. When the defect density keeps escalating, there is a heat dissipation route for the Joule heat generated at the interface, eventually achieving a dynamic thermal equilibrium state. At this point, the defect density at the interface reaches the upper limit. When the test times continue to increase, the current of the device will also reach the lower limit, and the current will stop decaying. When we delve further into this phenomenon and consider various scenarios in which these bilayer and trilayer devices are utilized under different conditions and stress factors such as varying voltage levels or environmental temperatures, it becomes obvious that their unique structure plays a crucial role in maintaining stability during operation.

3.4 Characterization of the stability of electrical performance in metal transfer devices

To safeguard monolayer WSe_2 devices against thermal effects, the metal transfer approach was utilized to establish vdw contacts rather than covalent bonds between the electrodes and WSe_2 flakes. Prior research has indicated that vdw contacts display conspicuously lower contact resistance, which contributes to suppressing thermal effects at the contact interface. The detailed transfer method has been presented in the Experimental section. Electrodes of silver (Ag, 4.26 eV) and gold (Au, 5.1 eV) with distinct work functions were successfully transferred onto monolayer WSe_2 flakes. Images of the transferred devices are

depicted in Fig. S9. The transfer characteristics of the metal transfer devices are illustrated in Fig. 5a, b. The results reveal that Ag-transferred devices presented bipolar transfer curves with a predilection for n-type behavior, suggesting a lower electron barrier than a hole barrier. In contrast, Au-transferred devices exhibited purely p-type semiconductor behavior due to their higher work function. These discoveries demonstrate that by modifying the work function of the contact metals, the dominant carrier type of the metal transfer devices can be systematically tailored from electrons to holes. This is primarily ascribed to the vdw contact interface between the metal electrodes and the semiconductor. The repeatability test of the metal-transferred devices is illustrated in Fig. 5c, d. The outcomes

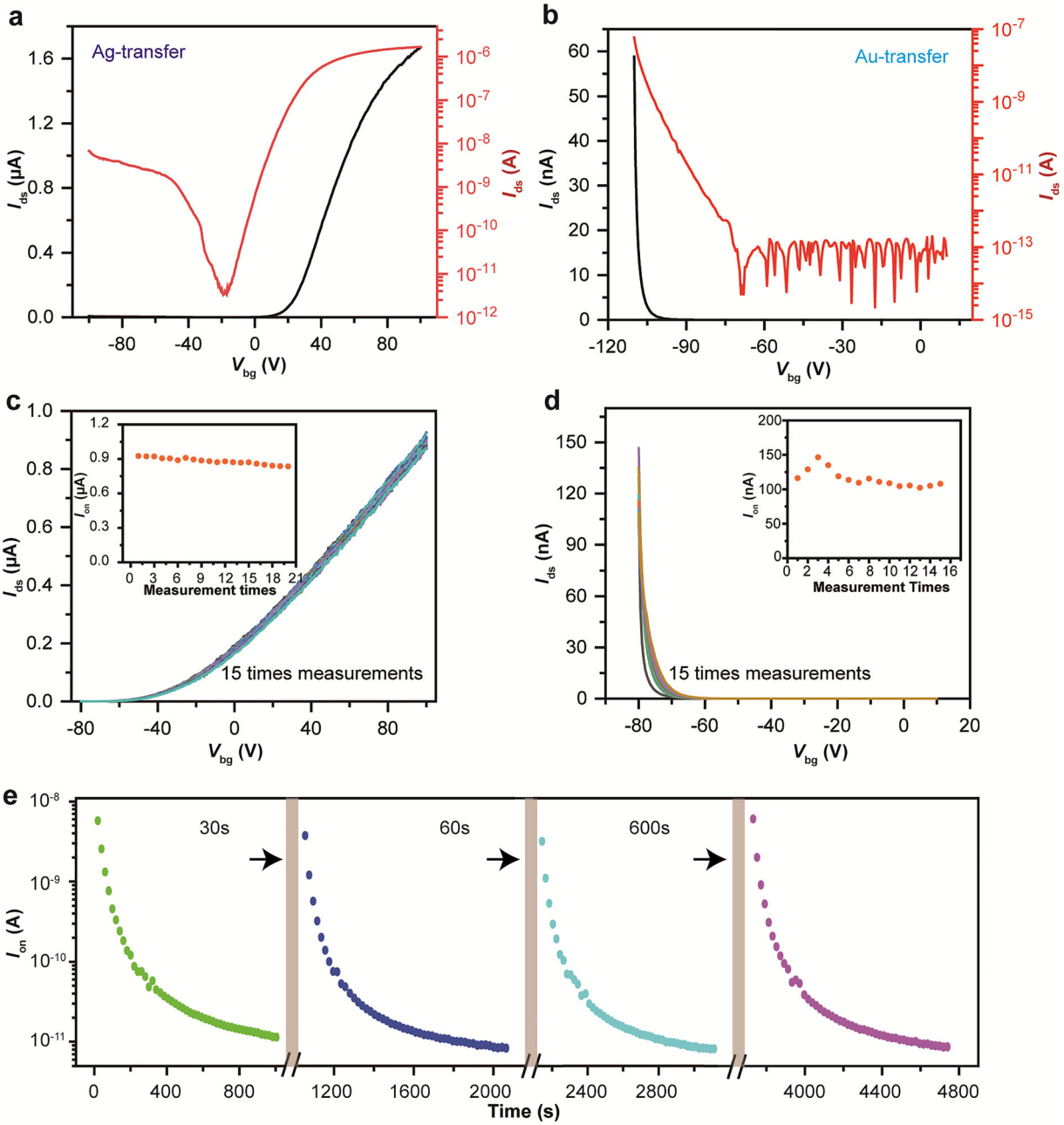

Fig. 5 Room-temperature electrical characteristics of metal-transferred monolayer WSe_2 devices under ambient environment: transfer characteristics on semilogarithmic (black) and linear (red) scales at a voltage bias of 0.1 V between source and drain electrodes for **a** Ag-transfer device and **b** Au-transfer device; transfer characteristics of **c** Ag-transfer and **d** Au-transfer devices under 15 times repeatability measurements and (inset) statistical information of I_{on} versus measurement times; **e** I_{on} versus time curves of monolayer Au transfer devices at V_{bg} = − 80 V and V_{ds} = 1 V (sampling frequency is 20 s, after working for 900 s, device is set to periods of quiescence, and period time is 30, 60 and 600 s, respectively)

suggested that the metal-transferred devices showcased remarkable gate control even after 15 measurements at room temperature. The statistics of I_{on} in the inset figures remained invariant with the varying numbers of measurements. It could be discerned from the results that, regardless of whether it is the n-type device with Ag transfer or the p-type device with Au transfer, the on-state current undergoes merely minor variations upon repeated tests. Compared with the repeatability test results of the monolayer device in Fig. 3 at room temperature, the metal-transferred devices possessed heightened stability. The current response of I_{on} versus time under V_{bg} = −80 V and V_{ds} = 1 V in an ambient environment was depicted in Fig. 5e. As the measurement time prolonged, I_{on} initially underwent a sharp decline. However, when the device was given a 30 s rest, the I_{on} could restore to 60% of the initial value during the second test, and I_{on} would decrease again with the increasing working time. Then, the second rest period was extended to 60 s after 900 s of working, and the result indicated that I_{on} could restore to 80%. Similarly, when the rest period was further prolonged to 600 s, I_{on} in the fourth test fully recovered to the initial value of the first test. For metal-transferred devices, vdw contact ensures lower contact resistance compared to covalent bond contact. While hole carriers flow across the contact interface, the thermal effect is not prominent. However, as the measurement time increases, the thermal effect becomes crucial due to heat accumulation, leading to a decrease in I_{on}. When the device is allowed to rest, the accumulated heat gradually dissipates with the increasing rest time. When the rest time reaches 600 s, the generated heat at the interface will be completely dissipated, and the electrical performance will be restored to the initial value. Although transition metals can establish ideal van der Waals contacts and guarantee that the device maintains outstanding performance during repetitive tests, it is crucial to note that, in contrast to evaporated devices, the performance of metal transfer devices is significantly weakened. Key electrical performance parameters, such as on-state current, mobility, and threshold voltage, all demonstrate considerable attenuation. This is mainly ascribed to the experimental process of metal transfer. During the transfer process, despite choosing the superior flexible substrate PDMS and the PS solution that causes less damage to the material, due to the monolayer characteristic of the WSe_2 material, considerable damage occurs and the defect density increases, ultimately leading to significant attenuation of the device's electrical performance. To solve this problem, the transfer process needs further optimization by selecting more appropriate substrates and solutions to minimize material damage.

4 Conclusion

In this study, we conducted a systematic study of the contact properties between WSe_2 films and metal electrodes. Different numbers of WSe_2 layers were synthesized through a vapor-phase evaporation technique, while their contact resistance with multiple electrodes was precisely measured using the TLM. Our analysis disclosed that, while the contact resistances of bilayer and trilayer WSe_2 devices are within the kilo-ohm range, monolayer devices exhibit evasive contact resistance due to a broad distribution of resistance values along the channel length. This phenomenon was ascribed to the thermal effect at the contact interface. Notably, devices with vdw contacts, fabricated by a metal transfer method, demonstrate a much more stable contact interface, with a considerably limited thermal influence. These findings illuminate the crucial role of contact resistance in the electronic performance of 2D material-based FETs. The insights obtained from this research emphasize the paramount significance of optimizing contact interfaces to enhance the performance of next-generation electronic and optoelectronic devices.

Acknowledgements This study was financially supported by the Science and Technology Innovation Council of Shenzhen (No. KQTD20170810105439418), the National Key R & D Project from Minister of Science and Technology, China (No. 2021YFB3200304), National Natural Science Foundation of China (Nos. 6237129, 52125205, U20A20166, 61805015 and 61804011), the Natural Science Foundation of Beijing Municipality (No. Z180011) and the Fundamental Research Funds for the Central Universities.

Declarations

Conflict of interests Cao-Feng Pan is an editorial board member for *Rare Metals* and was not involved in the editorial review or the decision to publish this article. All authors declare that there are no competing interests.

References

[1] Mak KF, Lee C, Hone J, Shan J, Heinz TF. Atomically thin MoS_2: a new direct-gap semiconductor. Phys Rev Lett. 2010; 105(13):136805. https://doi.org/10.1103/PhysRevLett.105.136805.

[2] Splendiani A, Sun L, Zhang YB, Li TS, Kim J, Chim CY, Galli G, Wang F. Emerging photoluminescence in monolayer MoS_2. Nano Lett. 2010;10(4):1271. https://doi.org/10.1021/nl903868w.

[3] Radisavljevic B, Radenovic A, Brivio J, Giacometti V, Kis A. Single-layer MoS_2 transistors. Nat Nanotechnol. 2011;6(3):147. https://doi.org/10.1038/Nnano.2010.279.

[4] Gao GY, Wan BS, Liu XQ, Sun QJ, Yang XN, Wang LF, Pan CF, Wang ZL. Tunable tribotronic dual-gate logic devices based on 2D MoS_2 and black phosphorus. Adv Mater. 2018;30(13): 1705088. https://doi.org/10.1002/adma.201705088.

[5] Ma W, Lu J, Wan B, Peng D, Xu Q, Hu G, Peng Y, Pan C, Wang ZL. Piezoelectricity in multilayer black phosphorus for

piezotronics and nanogenerators. Adv Mater. 2020;32(7):1905795. https://doi.org/10.1002/adma.201905795.
[6] Desai SB, Madhvapathy SR, Sachid AB, Llinas JP, Wang QX, Ahn GH, Pitner G, Kim MJ, Bokor J, Hu CM, Wong HSP, Javey A. MoS_2 transistors with 1-nanometer gate lengths. Science. 2016;354(6308):99. https://doi.org/10.1126/science.aah4698.
[7] Chhowalla M, Jena D, Zhang H. Two-dimensional semiconductors for transistors. Nat Rev Mater. 2016;1(11):16052. https://doi.org/10.1038/natrevmats2016.52.
[8] Lembke D, Bertolazzi S, Kis A. Single-layer MoS_2 electronics. Acc Chem Res. 2015;48(1):100. https://doi.org/10.1021/ar500274q.
[9] Lin J, Wang B, Yang ZY, Li GL, Zou XM, Chai Y, Liu XQ, Liao L. High-current MoS_2 transistors with non-planar gate configuration. Sci Bull. 2021;66(8):777. https://doi.org/10.1016/j.scib.2020.12.009.
[10] Gao G, Yu J, Yang X, Pang Y, Zhao J, Pan C, Sun Q, Wang ZL. Triboiontronic transistor of MoS_2. Adv Mater. 2019;31(7):1806905. https://doi.org/10.1002/adma.201806905.
[11] Liu H, Neal AT, Ye PDD. Channel length scaling of MoS_2 MOSFETs. ACS Nano. 2012;6(10):8563. https://doi.org/10.1021/nn303513c.
[12] Akinwande D, Huyghebaert C, Wang CH, Serna MI, Goossens S, Li LJ, Wong HSP, Koppens FHL. Graphene and two-dimensional materials for silicon technology. Nature. 2019;573(7775):507. https://doi.org/10.1038/s41586-019-1573-9.
[13] Allain A, Kang JH, Banerjee K, Kis A. Electrical contacts to two-dimensional semiconductors. Nat Mater. 2015;14(12):1195. https://doi.org/10.1038/nmat4452.
[14] Xu Y, Cheng C, Du SC, Yang JY, Yu B, Luo J, Yin WY, Li EP, Dong SR, Ye PD, Duan XF. Contacts between two- and three-dimensional materials: ohmic, schottky, and p-n heterojunctions. ACS Nano. 2016;10(5):4895. https://doi.org/10.1021/acsnano.6b01842.
[15] Leonard F, Talin AA. Electrical contacts to one- and two-dimensional nanomaterials. Nat Nanotechnol. 2011;6(12):773. https://doi.org/10.1038/Nnano.2011.196.
[16] Ho PH, Chang YR, Chu YC, Li MK, Tsai CA, Wang WH, Ho CH, Chen CW, Chiu PW. High-mobility InSe transistors: the role of surface oxides. ACS Nano. 2017;11(7):7362. https://doi.org/10.1021/acsnano.7b03531.
[17] Andrews K, Bowman A, Rijal U, Chen PY, Zhou ZX. Improved contacts and device performance in MoS_2 transistors using a 2D semiconductor interlayer. ACS Nano. 2020;14(5):6232. https://doi.org/10.1021/acsnano.0c02303.
[18] Zhang Y, Shang Z, Wang G, Wang X. Spin polarization of chiral molecules and electronic device applications. Chin J Rare Met. 2023;47(8):1163. https://doi.org/10.13373/j.cnki.cjrm.XY23030017.
[19] Liu Y, Guo J, Zhu EB, Liao L, Lee SJ, Ding MN, Shakir I, Gambin V, Huang Y, Duan XF. Approaching the schottky-mott limit in van der Waals metal-semiconductor junctions. Nature. 2018;557(7707):696. https://doi.org/10.1038/s41586-018-0129-8.
[20] Zhang Q, Zuo SL, Chen P, Pan CF. Piezotronics in two-dimensional materials. Infomat. 2021;3(9):987. https://doi.org/10.1002/inf2.12220.
[21] Zhou Q, Deng S, Gao A, Wang B, Lai J, Pan J, Huang L, Pan C, Meng G, Xia F. Triboelectric nanogenerator with dynamic electrode for geological disaster and fall-down self-powered alarm system. Adv Func Mater. 2023;33(52):2306619. https://doi.org/10.1002/adfm.202306619.
[22] Shi Z, Zhao H, Chen X, Wu G, Wei F, Tu H. Chemical vapor deposition growth and transport properties of MoS_2-2H thin layers using molybdenum and sulfur as precursors. Rare Met. 2022;41(10):3574. https://doi.org/10.1007/s12598-015-0599-x.
[23] LaGasse SW, Dhakras P, Watanabe K, Taniguchi T, Lee JU. Gate-tunable graphene-WSe_2 heterojunctions at the schottky-mott limit. Adv Mater. 2019;31(24):1901392. https://doi.org/10.1002/adma.201901392.
[24] Liu W, Li LF, Guo HW, Qadir A, Bodepudi SC, Shehzad K, Chen WC, Xie YH, Wang XM, Yu B, Xu Y. Approaching the collection limit in hot electron transistors with ambipolar hot carrier transport. ACS Nano. 2019;13(12):14191. https://doi.org/10.1021/acsnano.9b07020.
[25] Wu H, Liu Y, Deng ZY, Cheng HC, Li DH, Guo J, He QY, Yang S, Ding MN, Huang YC, Wang C, Huang Y, Duan XF. A field-effect approach to directly profiling the localized states in monolayer MoS_2. Science Bulletin. 2019;64(15):1049. https://doi.org/10.1016/j.scib.2019.05.021.
[26] Zhou K, Xu W, Yu Y, Zhai W, Shen C. Tunable and nacre--mimetic multifunctional electronic skins for highly stretchable contact-noncontact sensing. Small. 2021;17(31):2100542. https://doi.org/10.1002/smll.202100542.
[27] Wang Y, Kim JC, Wu RJ, Martinez J, Song X, Yang J, Zhao F, Mkhoyan A, Jeong HY, Chhowalla M. Van der waals contacts between three-dimensional metals and two-dimensional semiconductors. Nature. 2019;568(7750):70. https://doi.org/10.1038/s41586-019-1052-3.
[28] Yang LM, Majumdar K, Liu H, Du YC, Wu H, Hatzistergos M, Hung PY, Tieckelmann R, Tsai W, Hobbs C, Ye PD. Chloride molecular doping technique on 2D materials: WS_2 and MoS_2. Nano Lett. 2014;14(11):6275. https://doi.org/10.1021/nl502603d.
[29] Bang S, Lee S, Rai A, Duong NT, Kawk I, Wolf S, Chung CH, Banerjee SK, Kummel AC, Jeong MS, Park JH. Contact engineering of layered MoS_2 via chemically dipping treatments. Adv Func Mater. 2020;30(16):2000250. https://doi.org/10.1002/adfm.202000250.
[30] English CD, Shine G, Dorgan VE, Saraswat KC, Pop E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. Nano Lett. 2016;16(6):3824. https://doi.org/10.1021/acs.nanolett.6b01309.
[31] Wang W, Liu Y, Tang L, Jin Y, Zhao T, Xiu F. Controllable Schottky barriers between MoS_2 and permalloy. Sci Rep. 2014;4(1):6928. https://doi.org/10.1038/srep06928.
[32] Ma YG, Liu BL, Zhang AY, Chen L, Fathi M, Shen CF, Abbas AN, Ge MY, Mecklenburg M, Zhou CW. Reversible semiconducting-to-metallic phase transition in chemical vapor deposition grown mono layer WSe_2 and applications for devices. ACS Nano. 2015;9(7):7383. https://doi.org/10.1021/acsnano.5b02399.
[33] Kappera R, Voiry D, Yalcin SE, Branch B, Gupta G, Mohite AD, Chhowalla M. Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors. Nat Mater. 2014;13(12):1128. https://doi.org/10.1038/nmat4080.
[34] He J, Zhou R, Zhang Y, Gao W, Chen T, Mai W, Pan C. Strain-insensitive self-powered tactile sensor arrays based on intrinsically stretchable and patternable ultrathin conformal wrinkled graphene-elastomer composite. Adv Func Mater. 2022;32(10):2107281. https://doi.org/10.1002/adfm.202107281.
[35] Niu YT, Qing FZ, Li XS, Peng B. Inhomogeneous strain and doping of transferred CVD-grown graphene. Rare Met. 2022;41(5):1727. https://doi.org/10.1007/s12598-021-01912-z.
[36] Went CM, Wong J, Jahelka PR, Kelzenberg M, Biswas S, Hunt MS, Carbone A, Atwater HA. A new metal transfer process for van der Waals contacts to vertical Schottky-junction transition metal dichalcogenide photovoltaics. Sci Adv. 2019;5(12):eeax6061. https://doi.org/10.1126/sciadv.aax6061.
[37] Zhu R, Li Z, Deng G, Yu YQ, Shui J, Yu R, Pan C, Liu X. Anisotropic magnetic liquid metal film for wearable wireless electromagnetic sensing and smart electromagnetic interference

shielding. Nano Energy. 2022;92:106700. https://doi.org/10.1016/j.nanoen.2021.106700.
[38] Liu Y, Wu H, Cheng HC, Yang S, Zhu EB, He QY, Ding MN, Li DH, Guo J, Weiss NO, Huang Y, Duan XF. Toward barrier free contact to molybdenum disulfide using graphene electrodes. Nano Lett. 2015;15(5):3030. https://doi.org/10.1021/nl504957p.
[39] Chee SS, Seo D, Kim H, Jang H, Lee S, Moon SP, Lee KH, Kim SW, Choi H, Ham MH. Lowering the schottky barrier height by graphene/Ag electrodes for high-mobility MoS_2 field-effect transistors. Adv Mater. 2019;31(2):1804422. https://doi.org/10.1002/adma.201804422.
[40] Chen XL, Xia FN. Enabling novel device functions with black phosphorus/MoS_2 van der Waals heterostructures. Sci Bull. 2017;62(23):1557. https://doi.org/10.1016/j.scib.2017.11.009.
[41] Cong R, Qiao S, Liu J, Mi J, Yu W, Liang B, Fu G, Pan C, Wang S. Ultrahigh, ultrafast, and self-powered visible-near-infrared optical position-sensitive detector based on a CVD-prepared vertically standing few-layer MoS_2/Si heterojunction. Adv Sci. 2018;5(2):1700502. https://doi.org/10.1002/advs.201700502.
[42] Lee CS, Oh SJ, Heo H, Seo SY, Kim J, Kim YH, Kim D, Okello OFN, Shin H, Sung JH, Choi SY, Kim JS, Kim JK, Jo MH. Epitaxial van der waals contacts between transition-metal dichalcogenide monolayer polymorphs. Nano Lett. 2019;19(3):1814. https://doi.org/10.1021/acs.nanolett.8b04869.
[43] Choi H, Moon BH, Kim JH, Yun SJ, Han GH, Leep SG, Gul HZ, Lee YH. Edge contact for carrier injection and transport in MoS_2 field-effect transistors. ACS Nano. 2019;13(11):13169. https://doi.org/10.1021/acsnano.9b05965.
[44] Chu CH, Lin HC, Yeh CH, Liang ZY, Chou MY, Chiu PW. End-bonded metal contacts on WSe_2 field-effect transistors. ACS Nano. 2019;13(7):8146. https://doi.org/10.1021/acsnano.9b03250.
[45] Aiyiti A, Bai X, Wu J, Xu XF, Li BW. Measuring the thermal conductivity and interfacial thermal resistance of suspended MoS_2 using electron beam self-heating technique. Sci Bull. 2018;63(7):452. https://doi.org/10.1016/j.scib.2018.02.022.
[46] Zhou K, Zhao Y, Sun X, Yuan Z, Shen C. Ultra-stretchable triboelectric nanogenerator as high-sensitive and self-powered electronic skins for energy harvesting and tactile sensing. Nano Energy. 2020;70:104546. https://doi.org/10.1016/j.nanoen.2020.104546.
[47] Ueda A, Zhang YJ, Sano N, Imamura H, Iwasa Y. Ambipolar device simulation based on the drift-diffusion model in ion--gated transition metal dichalcogenide ransistors. NPJ Comput Mater. 2020;6(1):24. https://doi.org/10.1038/s41524-020-0293-x.